

(1a. Components and Performance of Processors, A Level Only Content)

Answer **all** the questions.

start	LDA	one
	OUT	
	LDA	zero
	OUT	
	LDA	count
	SUB	one
	STA	count
	BRP	start
	HLT	
one	DAT	1
zero	DAT	0
count	DAT	3

[3]

[2]

[1]

Question			Answer/Indicative content	Marks	Guidance
1	a		<ul style="list-style-type: none"> – An instruction can be fetched as the previous one is being decoded ... – ... and the one before that is being executed. – E.g. LDA Zero can be fetched, while OUT is being decoded and start LDA one is being executed. (1 per –)	3	
	b		<ul style="list-style-type: none"> – BRP could be followed by one of two possible instructions, which one will only be determined at execution – Meaning the wrong one may be fetched / decoded (1 per –)	2	
	c		<ul style="list-style-type: none"> – Clock speed – Cache Size – Number of cores (1 per max 1) 	1	
			Total	6	
2			Pipelining would allow one instruction to be fetched as the previous one is being decoded and the one before that is being executed.(1) For example OUT could be fetched (1). As there are no jump/branch instructions it pipelines well (as there is no need to flush the pipeline). (1)	3	Accept any valid example from the given code.
			Total	3	